6.3 A Dual-Antenna Phased-Array UWB Transceiver in 0.18μm CMOS

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Given the popularity of WiFi among mobile computing users, wireless connectivity among multiple consumer electronics (CE) devices will soon be demanded to enable convenience and mobility. Such applications, for example, streaming of multiple simultaneous video streams, require high bandwidth, robust transmission, and low power. Ultra-wideband (UWB) technology offers a solution for high-date-rate and short-range communication. The multi-band OFDM (MB-OFDM) Alliance proposal divides the available spectrum from 3.1 to 10.6GHz into sub-bands of 528MHz. The mandatory mode-1 device implements the three lowest bands from 3.1 to 4.8GHz and supports data rates as high as 480Mb/s. The low transmit power of -41.25dBm/MHz, as mandated by the FCC, limits the range of transmission. In addition, since potential out-of-band or in-band interferers due to WiFi or WiMax may have significantly higher power than the desired UWB channel, extended range and robust transmission in the presence of these interferers are highly desirable for these CE devices.

To achieve extended range and improved attenuation of interferers, the transceiver architecture uses antenna diversity and a tunable RF bandpass filter in the receiver calibrated for optimal selectivity. The dual-antenna transceiver architecture is shown in Fig. 6.3.1. The transceiver employs two transmit and receive antennas. Selection diversity is implemented on both transmit and receive sides by choosing the branch with the higher SNR, as determined by the accompanying baseband processor. Selection diversity gain is maximized for non-line-of-sight wireless channels. In addition to selection diversity, equal-gain combining using a two-path four-phased-array receiver is also employed [1]. The two received signals are combined with the optimal LO phase shift at the mixer output. In the case where a strong interferer is causing desensitization of the receiver, it can be suppressed by phase combining. With a line-of-sight (LOS) interferer, this scheme of interference cancellation in a two-path four-phased-array receiver is particularly effective.

To improve attenuation of out-of-band interferers, the receiver implements an on-chip tunable bandpass filter (BPF) at the LNA output, as shown in Fig. 6.3.2. The tunable BPF has a 4b switched-capacitor array to tune for optimal selectivity of the desired band. The inductor Q is chosen as a tradeoff between in-band flatness and out-of-band attenuation. This BPF together with the baseband LPF attenuates an interferer at 528MHz offset by 50dB. Optimal selectivity is obtained by calibrating the BPF to maximize the in-band signal gain and out-of-band interferer attenuation. Measurement of the full tunable range of the BPF across different frequencies can also be used to calibrate the BPF for maximum symmetry, flatness or out-of-band attenuation. Calibration of the BPF center frequency does not require additional circuitry such as amplitude detector or a PLL. Instead, calibration is achieved by injecting an RF signal into the BPF and down-converting it with the mixer to obtain a low-frequency signal, the amplitude of which is digitized by an ADC and a decision is fed back to the tunable BPF. In the specific case of maximizing the in-band gain at the center of each band, the LO signal is injected in the BPF through the loop-back path from TX to RX and a dc signal is obtained in the baseband output and digitized. There is no need for additional amplitude detection circuitry at the BPF, which would increase the loading even when it is powered down.

The differential LNA has a three-section network for broadband matching [2]. The LNA high gain is 19dB and the low gain is 2dB. The mixer is a double-balanced Gilbert cell with a conversion gain of 13dB. Band selectivity and automatic gain control (AGC) are performed by a 4th-order Chebyshev filter with a nominal cut-off frequency of 259MHz and the VGA stages, which are partitioned to achieve optimal noise and linearity performance. The VGA stages together with the gain control in the LNA achieve an overall gain range of 1 to 64dB in 1dB steps. DACs are placed along the receive chain to compensate for dc offsets.

The LO generation scheme, as shown in Fig. 6.3.3, has been designed to switch frequencies within the guard-interval specification of 9.5ns during band-hopping. Each mixer shown in the figure is a SSB mixer. The LO generation scheme was designed to avoid having the VCO frequency and the unwanted sidebands of the SSB mixers fall between 3.1 and 4.8GHz. The single PLL, together with the SSB mixers, dividers and multiplexers, generates all the required LO frequencies. The divide-by-two circuit following the VCO provides the four phases. The phase selection circuit is controlled by the baseband chip for optimal phase selection in dual-receiver mode.

The TX low-pass filter is designed to have a 4th-order Butterworth response with a nominal corner frequency of 310MHz. The filtered baseband signal is upconverted by a SSB double-balanced Gilbert-cell mixer. The inductive load at the output is optimally tuned to the desired band. A DAC introduces an offset current into the modulator to achieve LO leakage of less than -50dBm. A single modulator drives two power amplifiers (PAs) to achieve transmit selection diversity. Power detectors and an 8b ADC are integrated to calibrate TX output power and TX IQ gain and phase mismatch.

Figure 6.3.4 summarizes the measured results. Measurements are made on devices in a 56pin W-TAPP package mounted on a FR4 PCB. Figure 6.3.3 shows the switching behavior of the LO. The two receivers are matched in gain to within 1dB. Figure 6.3.5 shows the measured interference attenuation versus radiation angle. The measured pattern matches the theoretical results given a 1dB gain mismatch. The measured peak-to-null ratio is larger than 18dB.

Figure 6.3.6 shows that the transmit output spectrum is fully compliant with the FCC mask for UWB without any external BPF. The EVM was measured for 480Mb/s with an in-house tool on the TX output sampled by a high-speed digital oscilloscope. It meets the EVM specification of -19.5dB for 480Mb/s in the MBOA proposal. Figure 6.3.7 shows the die micrograph. The 4.2mm×3.8mm IC is fabricated in 0.18μm 1P6M CMOS. The chip consumes 412mW in receive mode and 397mW in transmit mode from 1.8V.

Acknowledgment:
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References:
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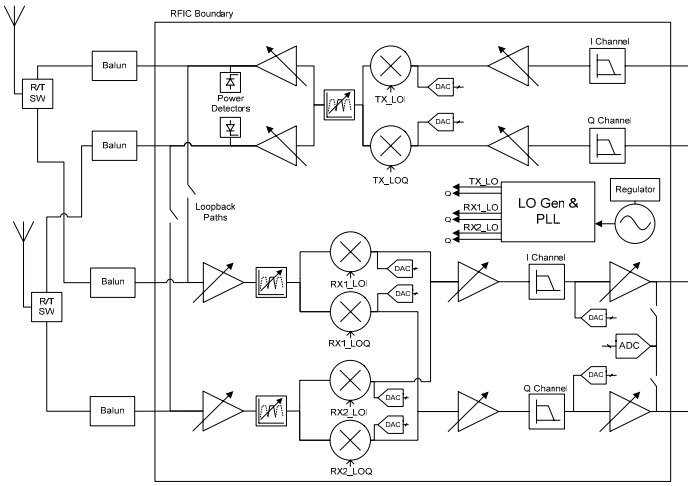

Figure 6.3.1: Transceiver architecture.

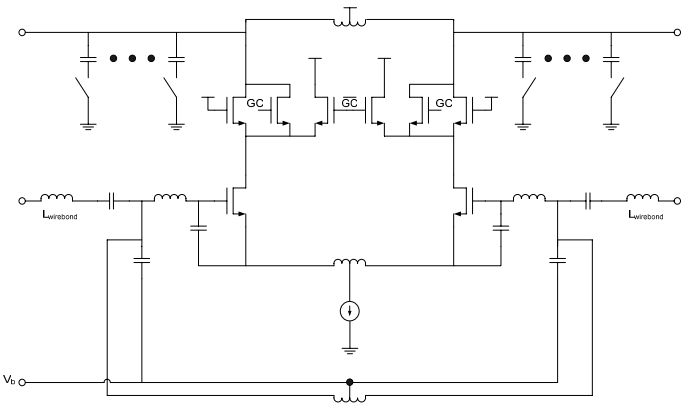

Figure 6.3.2: Low-noise amplifier.

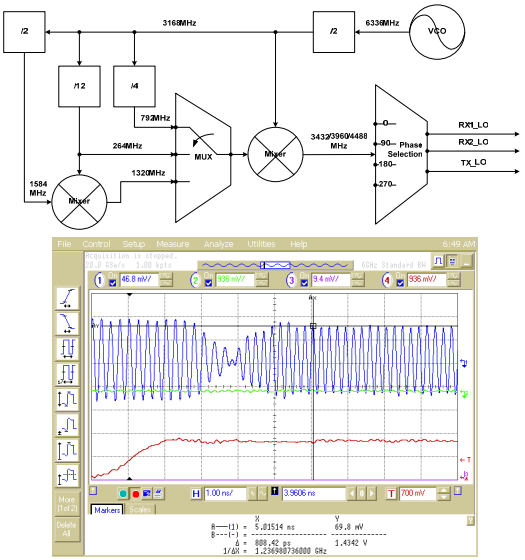

Figure 6.3.3: Block diagram of local oscillator generation scheme and switching time.

Center Freq (Mhz)	3432	3960	4488
Rx Voltage Gain (dB)	63.8	63.6	62.7
Noise Figure (dB)[1]	4.0	4.4	4.7
S11 (dB)	-14.7	-14.4	-13.2
In-band IIP3 (dBm)[2]	4.2	-0.8	0.5
In-band P1dB (dBm)[2]	-5	-8	-9
In-band IIP2(dBm)[2]	23.4	22	24.5
Blocker P1dB[3]	-8.7	-10.4	-8.7
Gain Control Range	61	60.7	60.9
VCO Phase noise at 1MHz (dBc/Hz)	-119	-118	-117
Spurious Tones (dBc)	36	44	43
Band-switching Settling Time (nsec)	5	5	5
Integrated rms error (deg)[4]	1.0	1.1	1.3
Tx Output Power (dBm)[5]	-12.6		
TX OP1dB (dBm)	3.9	3.1	4.7
TX OIP3 (dBm)	12	15.7	11.8
TX EVM (dB)	-28.6	-28.3	-27.2
Power Consumption (mW)			
RX-Single	412		
RX-Dual	527		
TX-Single	397		
TX-Dual	435		

[1] Noise figure is averaged across each band.
[2] In-band IIP3, P1dB and IIP2 were measured when receiver was set at minimum gain.
[3] Blocker frequencies are 2.4GHz, 3.5GHz and 5.1GHz. Worst-case blocker P1dB is reported for each band.
[4] Integrated rms error was measured from 10KHz to 300MHz.
[5] TX output power was measured in frequency hopping mode.

Figure 6.3.4: Performance summary.

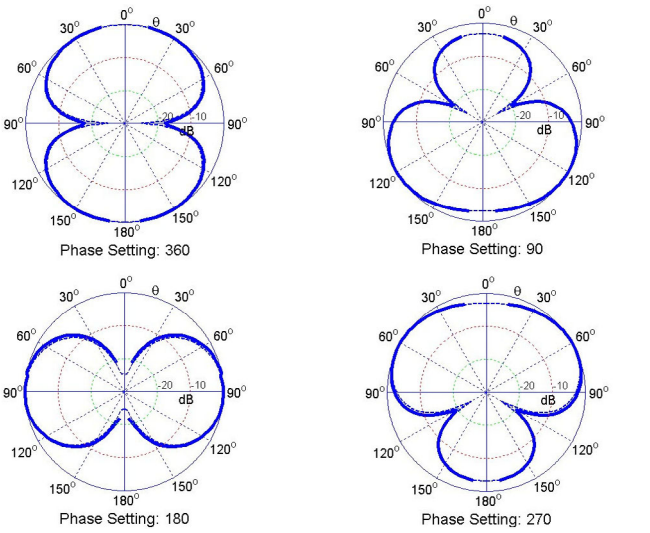

Figure 6.3.5: Theoretical (dotted lines) and measured (solid lines) interference rejection patterns.

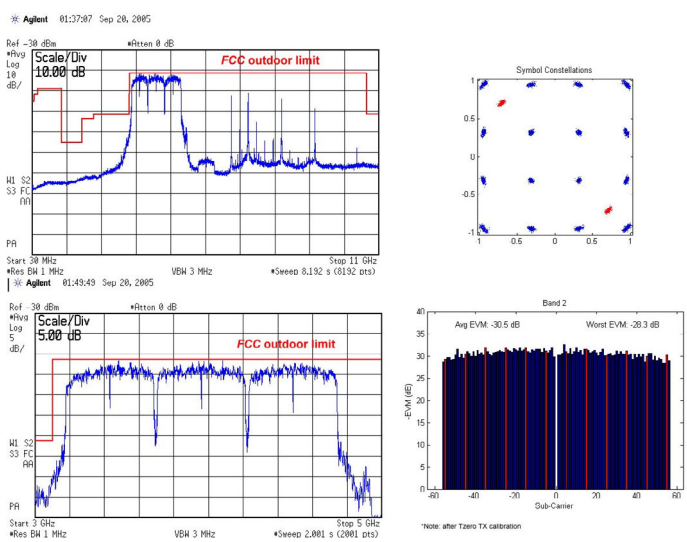

Figure 6.3.6: Measured transmit constellation and EVM for 480Mb/s.

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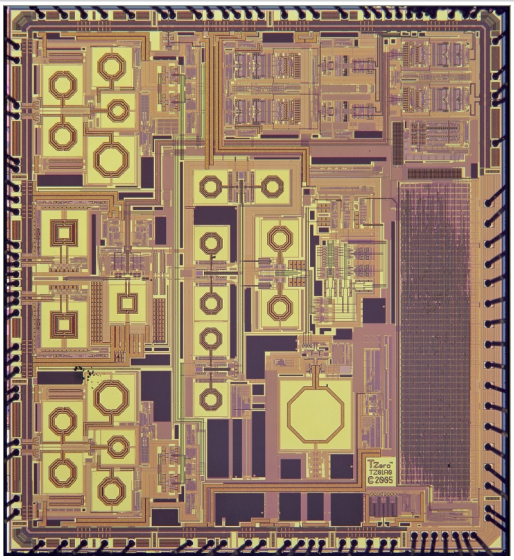

Figure 6.3.7: Chip micrograph.

